

60V(D-S) N-Channel Enhancement Mode Power MOS FET

**General Feature**

- $V_{DS} = 60V, I_D = 100A$   
 $R_{DS(ON)} < 6.5m\Omega @ V_{GS} = 10V$  (Typ: 5.7m $\Omega$ )
- Special process technology for high ESD capability
- High density cell design for ultra low Rdson
- Fully characterized Avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation



**Lead Free**

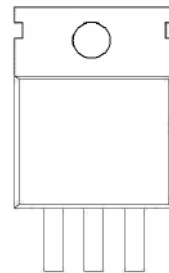
**Application**

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

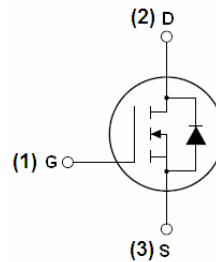
**PIN Configuration**



TO-220-3L top view



Marking and pin assignment



Schematic diagram

**Package Marking and Ordering Information**

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
MSN06B0K	MSN06B0K	TO-220-3L	-	-	-

**Absolute Maximum Ratings ( $T_C = 25^\circ C$  unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	100	A
Drain Current-Continuous( $T_C = 100^\circ C$ )	$I_D(100^\circ C)$	70	A
Pulsed Drain Current	$I_{DM}$	320	A
Maximum Power Dissipation	$P_D$	170	W
Derating factor		1.13	W/ $^\circ C$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	550	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ C$

**Thermal Characteristic**

Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta jc}$	0.88	$^{\circ}\text{C}/\text{W}$
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**Electrical Characteristics ( $T_C=25^{\circ}\text{C}$  unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	60	65	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=60V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <sup>(Note 3)</sup>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2	3	4	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=40A$	-	5.7	6.5	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=10V, I_D=40A$	-	50	-	S
<b>Dynamic Characteristics</b> <sup>(Note 4)</sup>						
Input Capacitance	$C_{iss}$	$V_{DS}=30V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	4800	-	PF
Output Capacitance	$C_{oss}$		-	440	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	260	-	PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=30V, I_D=1A$ $V_{GS}=10V, R_{GEN}=2.5\Omega$	-	16.8	-	nS
Turn-on Rise Time	$t_r$		-	10.8	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	55	-	nS
Turn-Off Fall Time	$t_f$		-	13.6	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=30V, I_D=30A,$ $V_{GS}=10V$	-	85	-	nC
Gate-Source Charge	$Q_{gs}$		-	18	-	nC
Gate-Drain Charge	$Q_{gd}$		-	28	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	$V_{SD}$	$V_{GS}=0V, I_S=20A$	-	-	1.2	V
Diode Forward Current <sup>(Note 2)</sup>	$I_S$	-	-	-	90	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^{\circ}\text{C}, I_F = 40A$ $di/dt = 100A/\mu s$ <sup>(Note 3)</sup>	-	38	-	nS
Reverse Recovery Charge	$Q_{rr}$		-	53	-	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

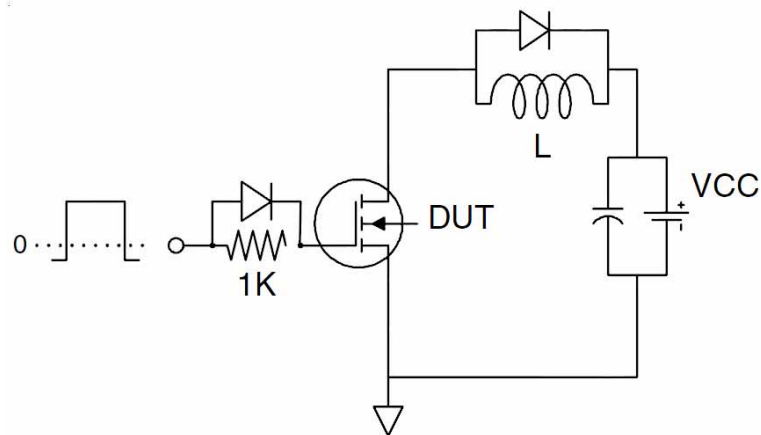
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5. EAS condition:  $T_J=25^{\circ}\text{C}, V_{DD}=30V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega$

**Test circuit**

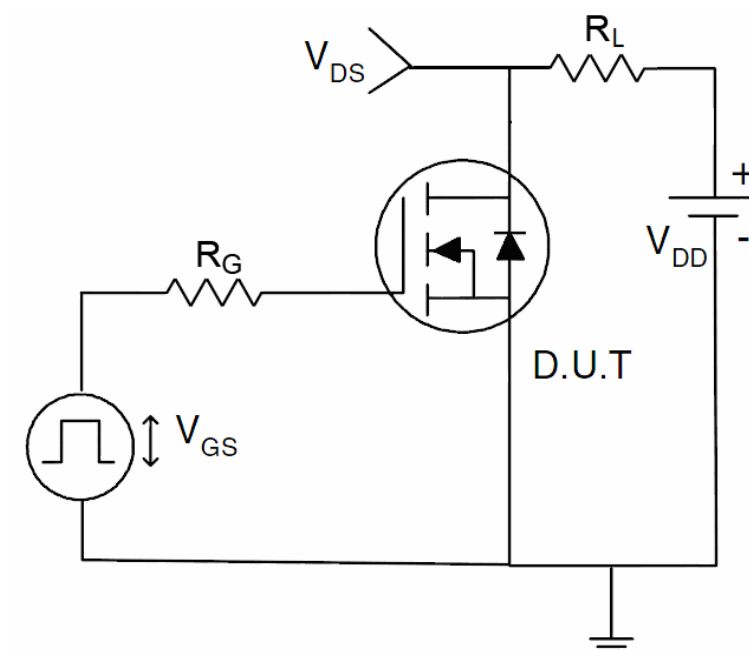
**1) E<sub>AS</sub> test Circuits**



**2) Gate charge test Circuit:**



**3) Switch Time Test Circuit:**



Typical Electrical and Thermal Characteristics (Curves)

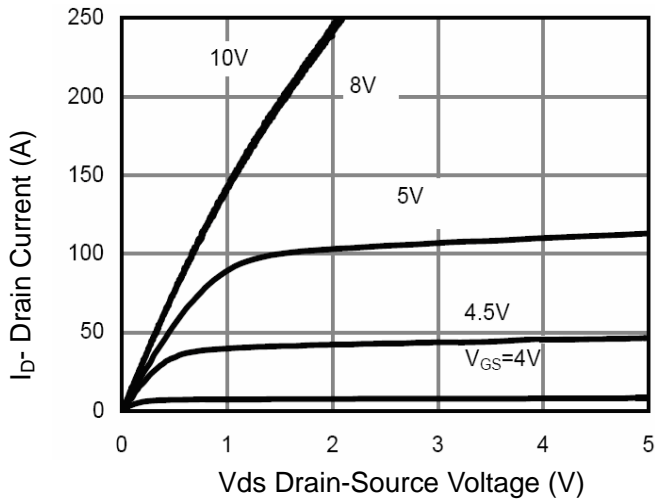


Figure 1 Output Characteristics

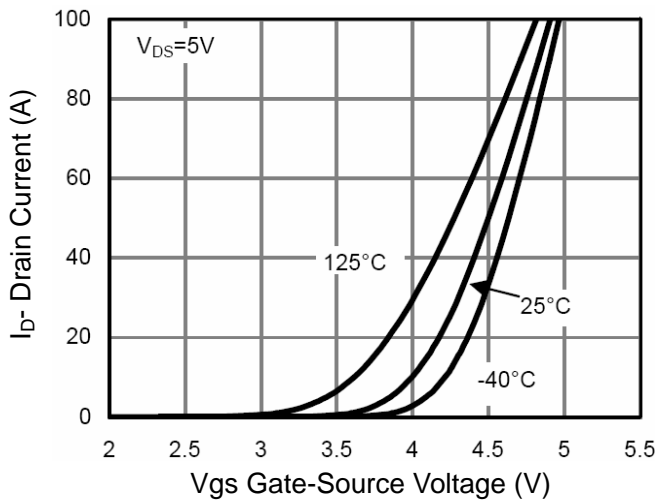


Figure 2 Transfer Characteristics

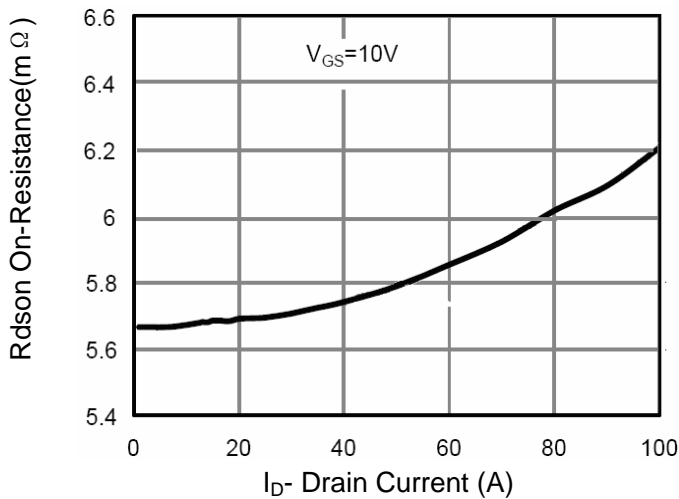


Figure 3 Rdson- Drain Current

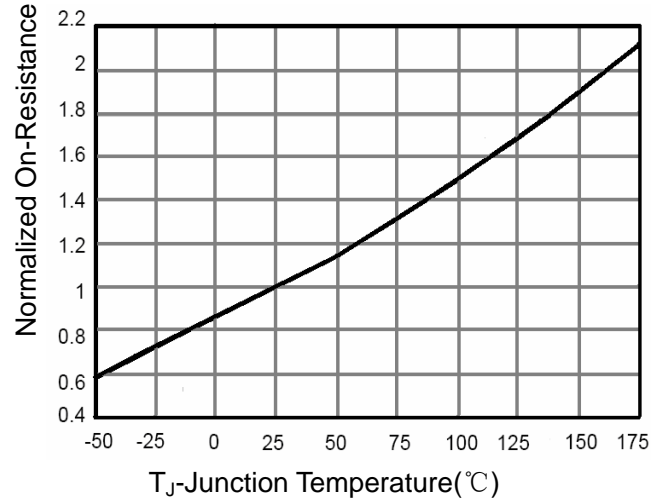


Figure 4 Rdson-Junction Temperature

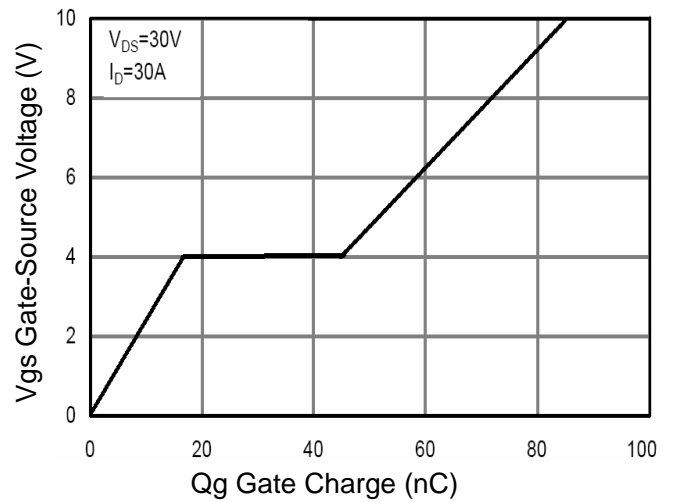


Figure 5 Gate Charge

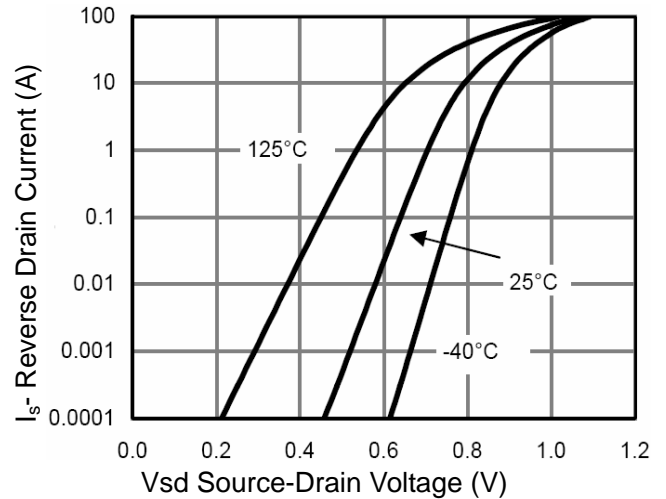


Figure 6 Source- Drain Diode Forward

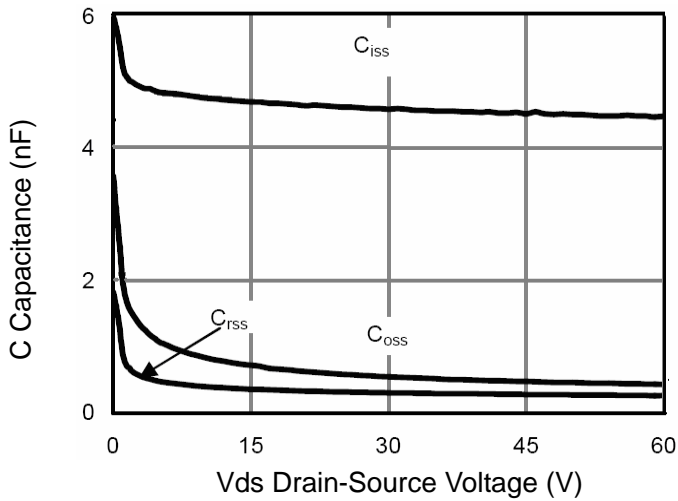


Figure 7 Capacitance vs Vds

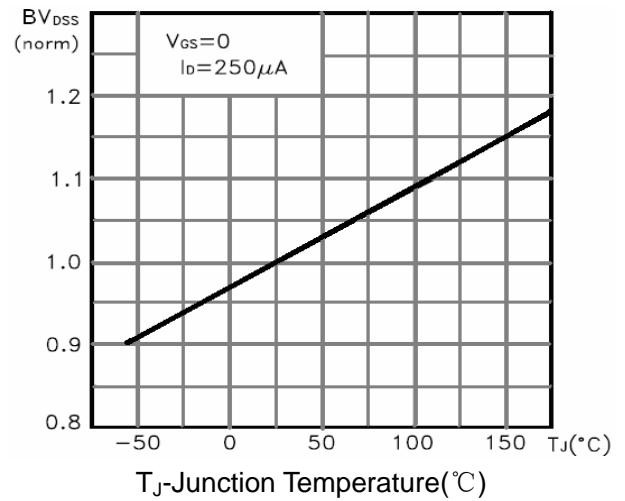


Figure 9  $BV_{DSS}$  vs Junction Temperature

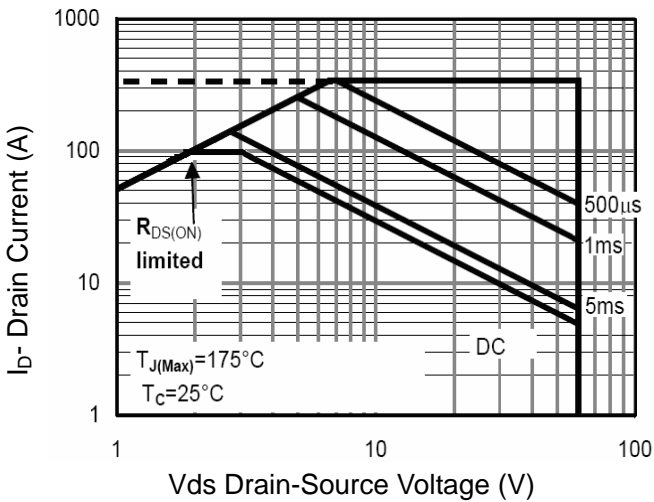


Figure 8 Safe Operation Area

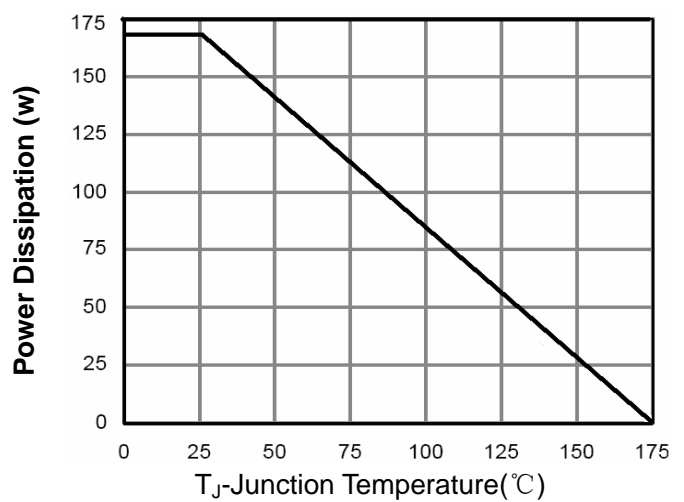


Figure 10 Power De-rating

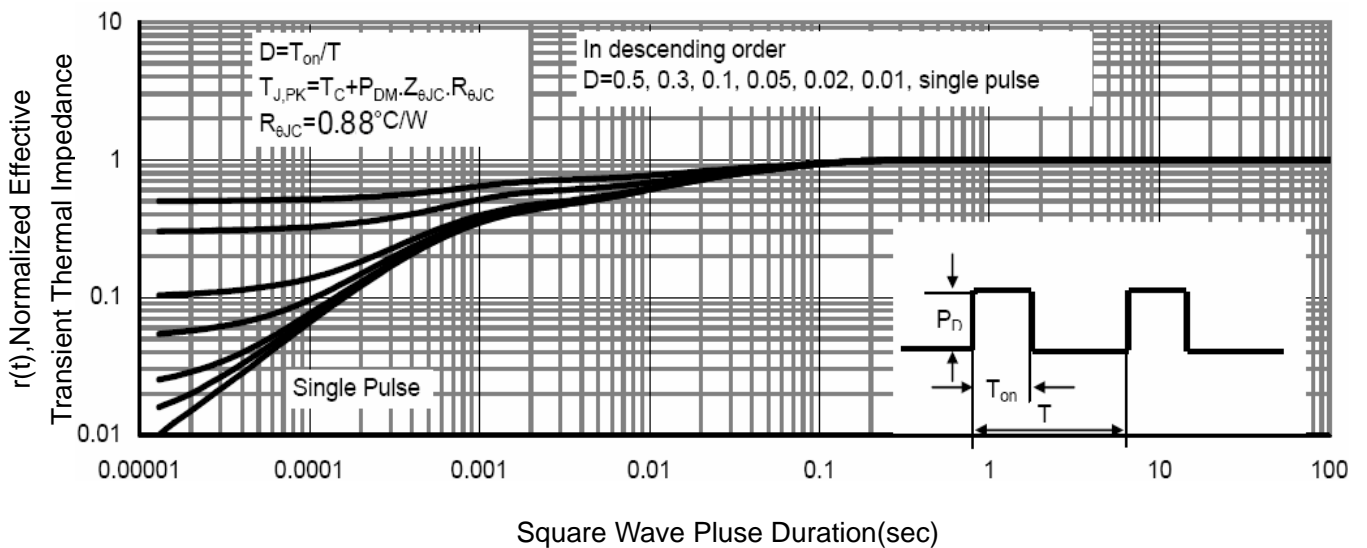
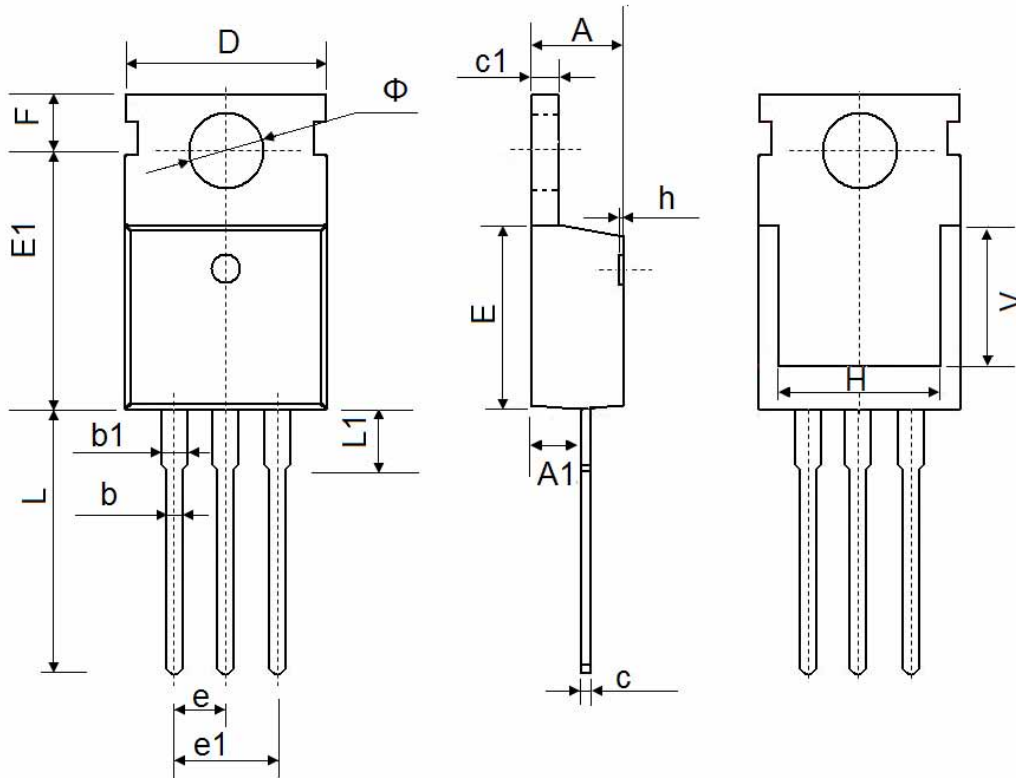


Figure 11 Normalized Maximum Transient Thermal Impedance

TO-220-3L Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.400	4.600	0.173	0.181
A1	2.250	2.550	0.089	0.100
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.330	0.650	0.013	0.026
c1	1.200	1.400	0.047	0.055
D	9.910	10.250	0.390	0.404
E	8.9500	9.750	0.352	0.384
E1	12.650	12.950	0.498	0.510
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.650	2.950	0.104	0.116
H	7.900	8.100	0.311	0.319
h	0.000	0.300	0.000	0.012
L	12.900	13.400	0.508	0.528
L1	2.850	3.250	0.112	0.128
V	7.500 REF.		0.295 REF.	
Φ	3.400	3.800	0.134	0.150